Moving Beyond 3D Hetero-Integration and Towards Monolithic Integration of Phase-Change RF Switches with SiGe BiCMOS

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Abstract: *A chip-scale, highly-reconfigurable transmitter and receiver, which hetero-integrates Northrop Grumman's novel phase-change switch (PCS) technology with commercial SiGe BiCMOS using 3D-stacking has been demonstrated. Further miniaturization and performance improvements are being pursued through fully monolithic integration. The current state of the technology will be discussed followed by a discussion of the advantages, goals and challenges of fully monolithic integration.*

Keywords: Phase-Change Switch (PCS); germanium telluride (GeTe); Low Loss RF switch; reconfigurable system; non-volatile switch; heterogeneous integration

Introduction

Northrop Grumman Electronic Systems (NGES) continues to advance a novel phase-change microelectronics technology that enables reconfigurable wideband RF systems for EW, RADAR and communications applications up to 40GHz. Because of its low loss and non-volatile operation, inline phase-change switch (IPCS) technology allows for larger-scale reconfigurable systems that are easily adaptable to changing mission needs. Below we discuss how the technology has been used in a chip-scale, reconfigurable receiver demonstration and ongoing efforts to increase the level of performance and practicality through further miniaturization and integration.

Technical Summary

Figure 1 shows our current approach to a highly reconfigurable RF circuit (RF-FPGA). It consists of a heterogeneous assembly of a SiGe BiCMOS chip with multiple 3D-integrated, low-loss, phase-change switch chiplets. The SiGe BiCMOS contains banks of RF components (amplifiers, mixers, vector modulators, filters) and digital logic as well as pulsers that can individually actuate the phase-change switches. The phase-change switch chiplets are passive multi-port (4- and 8-way) omnidirectional RF switches. The particular chip shown in Figure 1 is a reconfigurable receiver, containing 5 amplifiers, 2 IF down converters, 1 baseband down converter, 2 vector modulators and 7 band-pass filters with frequency coverage from 0.1 to 18GHz. Thirteen 8-way and two 4-way phase-change switch chiplets allow for a large number of arbitrary ways to configure the electrical paths between components in response to digital commands. The SiGe chip is 9mm on a side, while the 4- and 8-way switch chiplets are 1.3 and 1.7mm, respectively. Not including any components, there are greater than 800 possible unique ways to connect the RF input to the RF output, while passing through a minimum of 4 switch chiplets or a maximum of 12. Two possible ways that would result in a full receiver system (RF-to-baseband) are shown in Figure 2.

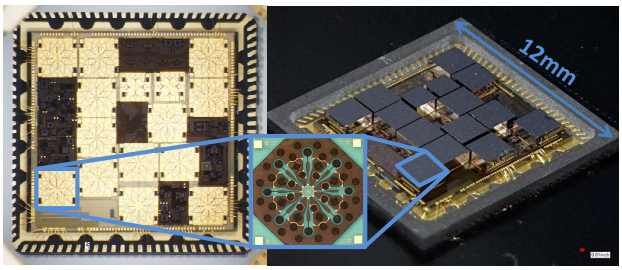

Figure 1. Left: SiGe chip in QFN not populated with switch chiplets; Center: Front-side view of 8-port PCS chiplet; Right: Optical photograph of a fully assembled receive RF-FPGA in QFN package.

Basic functionality of the RF-FPGA has been demonstrated, such as the ability to toggle individual switches on and off using commands supplied via the SiGe chip's digital logic circuits and the successful configuration of different paths resulting in different gains. While the current demo suffices for proving out the concept, it also comes with undesirable limitations that can easily be overcome with the size and performance advantages offered by fully monolithic integration.

In the current approach, the flip-chip integration imposes minimum size constraints on the switch chiplet due to mechanical constraints (handling and structural integrity) and due to a relatively large electrical interconnect section (per switch) that is required to achieve good electrical match and isolation within the integrated SiGe/PCS assembly. Figure 3 demonstrates the size savings that can be achieved by moving to a fully monolithic approach on the silicon base substrate of the SiGe BiCMOS process.

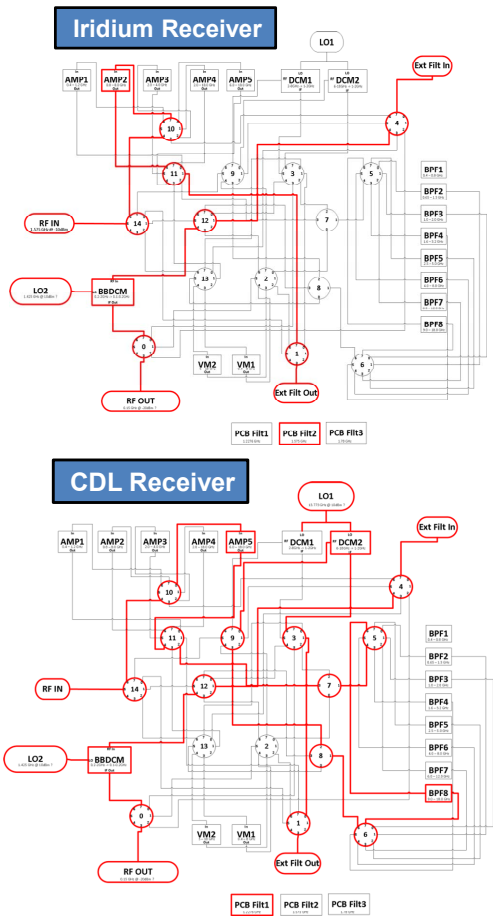

Figure 2. Interconnect diagram of receive RF-FPGA highlighting two system paths, namely, Iridium (top) and CDL (bottom).

Note from the circuit-side view of an 8-port switch chiplet (Figure 3, top-right) that the active PCS area is very small, around 1% of total chiplet area. This is because the phase-change switches are micron-scale devices (~30um on a side). The remaining features on the chiplet (transmission lines, bumps, alignment structures) serve only the purpose of ensuring mechanical and electrical integrity when the chiplet is integrated to the SiGe chip. In the current approach, the chiplet area is dominant compared to the active area on the SiGe die. By going to a fully monolithic approach, the switch area can be greatly reduced (up to 52%), which would allow for an increase in active area on the SiGe die enabling more functionality. Alternately, a roughly 2X reduction in size of the RF-FPGA chip can be achieved with the same level of functionality. The goal of monolithic integration would be to achieve maximum system cost benefit through a combination of reduced size and increased functionality.

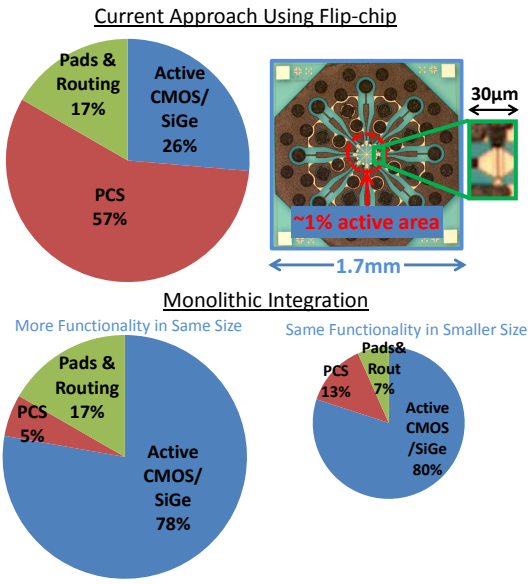

Figure 3. Size/performance advantages of a fully monolithic approach integrating SiGe BiCMOS with PCS compared to a flip-chip approach. A ~50% increase in functionality for the same size or a 2X decrease in size for the same functionality can be realized.

Another goal of monolithic integration is to be as process-agnostic as possible in order to maximize the cost benefit. A process-agnostic integration approach allows for the flexibility to integrate with new or existing designs in RF-CMOS, or SiGe BiCMOS from any foundry. The only way to accomplish this is to do a back end of line integration (i.e. a post-processing approach), and herein lies the challenge: the thick, metal-interconnect supporting oxide that is present on all CMOS device wafers poses a challenge to PCS device operation by slowing down the quench time and potentially preventing the switch from turning off (Figure 4). Note, that in order to successfully turn off (amorphize) the PCS using a 100ns actuation pulse, the GeTe material must follow a cooling trajectory that passes through the green-shaded box in Figure 4. However, simulations show that the thickness of oxide present on CMOS wafers places this trajectory at the edge of the boundary, potentially making it inoperable. Inoperability due to insufficient quench has, in fact, been confirmed experimentally on thick layers with very poor thermal conductivity.

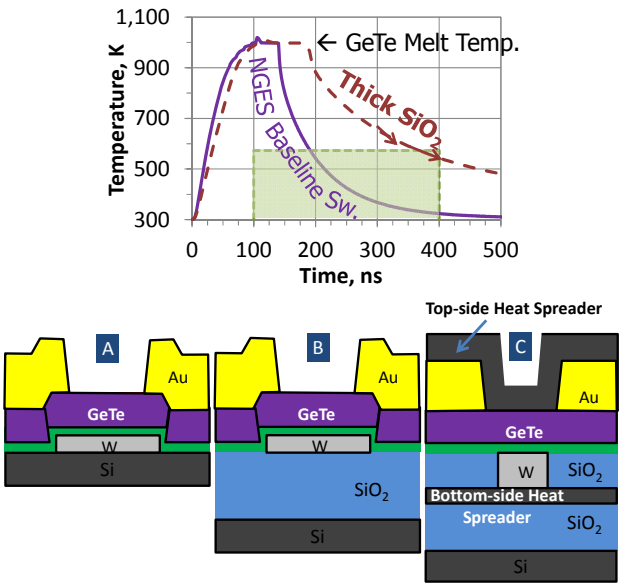

Figure 4. Simulated heat/quench profile of a NGES baseline phase-change switch (stackup A) and a switch post-integrated onto CMOS (stackup B). Structure for monolithic integration with CMOS, consisting of a high aspect ratio, damascene heater structure and heat spreader(s) (stackup C).

To overcome this challenge, a heat spreader (or layer with high thermal conductivity and appropriate thickness) is required to speed up the quench (Figure 4). A top-side, bottom-side or both types of heat spreaders may be used within the same structure, with top-side-only preferred because it is least disruptive to the overall switch process flow.

Since the power to amorphize is mostly dictated by the volume of GeTe above the heater, it is possible to tweak the ratio of actuation voltage to current by making the heater thicker or shallower, in turn changing its resistance. The goal is to lower the actuation voltage to a level that is compatible with a MOSFET driver circuit in the CMOS process, which may be on the order of ~5V. For the thickness required to achieve this, the structures with non-damascene heaters (Figure 4, A and B) would be very difficult, if not impossible to fabricate, due to step discontinuity coverage issues. This is because it is desired to keep the heater width as small as possible (<0.5μm) to reduce parasitic coupling, while making it as thick as possible to keep the heater resistance low. Therefore, the damascene structure, as shown in Figure 4C, is preferred.

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